Thin Flexible Crystalline Silicon for Photovoltaics

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ABSTRACT

Preliminary results of a Silicon-On-Insulator to polymer transfer technique capable of producing large area flexible crystalline silicon layer of thicknesses between 0.4 and 2.0 µm, are presented. Formation of a shallow pn junction using ion implantation of Phosphorus was confirmed through capacitance-voltage measurements with further analysis of these results revealing a sharp junction definition. Further to these results, photocurrent spectroscopy measurements show a clean photo-response, indicative of highly crystalline doped silicon. The results presented show that there is great promise for this transfer technique in the fabrication of thin flexible silicon devices, with the observed photo-response further suggesting using this process for production of flexible photovoltaic devices. Some of the issues with production of such devices over large surface areas, as well as device design issues are discussed, along with some measurements that should be performed to give a better understanding of the performance of these devices under varying conditions.

Keywords  Thin film, flexible, silicon, photovoltaics

INTRODUCTION

Thin film solar cells have been of interest for many years for driving down the cost of photovoltaics, with a broad range of materials used now for achieving high efficiencies (Wu et al. 2001, Repin et al. 2008, Bauhuis et al. 2009) and even flexible multijunction devices (Takamoto et al. 2006). Despite this success, the material quality available from the low temperature processing used in most thin film approaches means the efficiencies fall well short of those possible in monocrystalline devices (Basore 1999, Bergmann et al. 2001, Green et al. 2010). With a growing interest in building integrated (Gutscher 2002), and portable photovoltaics (DARPA 2009), the ability to fabricate flexible solar cells with efficiencies above those possible with amorphous or polycrystalline materials is of growing interest.

Recently, there have been reports of the use of thin flexible and crystalline silicon fabrication for realizing a number of novel electronic and optoelectronic devices (Liu et al. 2002, Menard et al. 2004, Roberts et al. 2006, Yuan & Ma 2006, Yuan et al. 2006,Yuan et al. 2009, Kim & Rogers 2009). One of the reports has even shown a flexible silicon photovoltaics panel with a reported energy conversion efficiency of up to 11.6 % and bending radii down to 4.9 mm (Yoon et al. 2009). The fabrication of these flexible silicon devices is dependent on pre-patternning of transfer substrates adding to the complexity and ultimately the cost of fabrication.
A simple process for obtaining large area thin flexible silicon layers from SOI substrates using a dual TMAH step process without the need for pre-patterning, is reported in this article. Good quality \textit{pn} junctions have been formed in these flexible silicon layers, and opening up the possibility of flexible silicon photovoltaic devices. We present some initial results for these thin silicon layers and also discuss some of the issues for realising photovoltaic devices using this approach.

**THIN FLEXIBLE SEMICONDUCTUR LAYERS**

Recently there have been a number of reports of the successful fabrication of various electronic and optoelectronic devices on flexible polymer substrates using Group IV semiconductors. The devices fabricated include thin film transistors (Menard et al. 2004) as well as photodetectors (Yuan et al. 2009) and even silicon solar cells (Yoon et al. 2009). Generally speaking the fabrication of these devices is achieved by transferring a thin semiconductor surface layer from a silicon-on-insulator or germanium-on-insulator (GOI) substrate to a flexible polymer substrate. The method of the transfer of the thin semiconductor layer (often referred to as a nanomembrane due to the thinness) has typically consisted of an etching treatment followed by mechanical force in order to detach from the underlying substrate and fix to the flexible platform. A critical feature of all of the fabrication procedures is the use of a pre-transfer patterning step of the thin semiconductor layer. The reason for this step is two-fold with structures being easier to pattern when the thin layer is still attached to a rigid substrate and the Buried Oxide (BOX) layer underneath being exposed to allow selective etching for detachment.

**Large Area Transfer Process**

A simple large area substrate-transfer process to deposit the thin device layer of commercial SOI wafers onto flexible polymer substrates has been developed. By replacing the standard HF-based transfer process by a dual-step TMAH-based process we have been able to transfer up to 4 \( \mu \)m-thick crystalline silicon films onto flexible substrate. This constitutes a major improvement since increasing the thickness allows one to form more “conventional” thin-film \textit{pn} junction structures and therefore might lead to much higher efficiencies. Most importantly, this process allows the inconvenient pre-patterning step often required to allow transfer using the HF-based process previously described by Rogers’ and Lagally’s group to be circumvented and for larger area devices to be fabricated, reducing interconnects on a per metre basis.

To transfer the flexible silicon layer onto a polyethylene terephthalate (PET) substrate, we start with a pristine piece of silicon-on-insulator (SOI) wafer having a device layer between 0.4 and 2.0 \( \mu \)m thick and a 500 nm-thick buried-oxide layer. The ProTEK B3 primer and the polymer are spin-coated on the SOI at 1500 rpm for 60 seconds. The sample is then baked first at 140 C for 2 min and then at 205 C for 1 min. The same primer and polymer coatings are also applied on a \( \sim 0.19 \) mm-thick cover glass using the same process and bonded to the protected device layer of the SOI before a subsequent baking. The protected SOI wafer is then back-etched in 30% KOH aqueous solution at 80 C for 7.5 hours to remove most of the exposed 625 \( \mu \)m-thick Si handle.

The sample is then cleaned in de-ionized water and transferred into a bath of 25 \% TMAH at 90 C to finalize the Si handle removal. Once the handle is completely etched, the oxide layer is removed using 49\% HF at room temperature for \( \sim 30-60 \) seconds, a process that only partially etches the glass slide. The exposed side of the device layer now supported by the cover glass slide is bonded to a flexible PET substrate (Sigma-
Aldrich part.636924) and HF etching is used to etch off the remainder of the cover glass support. Finally, the ProTEK film protecting the device layer is removed using the ProTEK 100 Remover to leave a large-area thin (0.4 - 2.0 µm) Si membrane attached to the flexible PET substrate. A pictorial summary of the process flow is shown in Figure 1 below.

Figure 1: Process flow for the transfer of thin crystalline silicon films onto flexible PET substrates using standard processing techniques and simple mechanical transfer techniques. Note the lack of pre-patterning required for the definition of devices.
RESULTS

Using the process outlined in the previous section, 1 cm\(^2\) layers of flexible silicon of thicknesses between 0.4 µm and 2.0 µm were transferred to PET substrates. This area was determined by the size of the glass slide being used as a mechanical support and it is expected that much larger areas can be easily obtained. As can be seen in Figure 2 a), these structures could be easily bent, to radii of curvature below 1 cm. This is due to the flexibility of the PET substrate and the fact the silicon is so thin that the rigidity we normally associate with silicon is not present and it appears more as high gloss paint. In order to confirm that the thin flexible silicon layers remained crystalline after the transfer confocal Raman micro-spectroscopy measurements were performed with the structure both planar and in bent mode.

The micro-Raman setup consisted of a Jobin-Yvon confocal microscope fibre coupled to a triple-grating spectrometer equipped with a Synapse TE-cooled detector array. The excitation is performed using a 532 nm frequency-stabilized TORUS laser (from Laser Quantum) and the power delivered to the sample is 15 mW. The Raman or Stokes shift in the emitted light was found to be sharp for both cases with the results for a layer with a bend radius of curvature of 5 mm displayed in Figure 2 b). Also shown in Figure 2 c) is the experimental arrangement used in order to enhance the Raman signal. It relies on Ag nano-particles printed using an anodic Aluminium etched mask and is described elsewhere (Nataraj & Cloutier 2010). Finally in Figure 2 d) the location of the Raman peak as a function of the radius of curvature is shown along with the strain of

![Figure 2: Flexible silicon on polymer structure; a) photograph of a typical 2 µm thick flexible crystalline silicon layer on a polymer substrate produced using the SOI-to-polymer technique described in the text. b) Result from confocal Raman micro-spectroscopy study of a transferred silicon layer under maximum bending of 5 mm radius of curvature. c) use of array of Ag particles for surface enhanced Raman effect. d) variation of Raman peak position with bending of flexible silicon and hence strain.](image-url)
the bent layer. We see that the bending needs to be quite severe (below 2 cm radius of curvature) to see an appreciable shift in the Raman signal. This indicates that even when the layer is bent quite severely the crystallinity of the silicon is preserved, since a narrow phonon mode is being observed in these measurements.

In order to obtain *pn* junctions in the silicon layers prior to transfer from the SOI wafer the layer underwent ion implantation with $^{31}\text{P}^+$ ions. The choice of P as the *n* type dopant was justified on the basis of predicted doping profiles in silicon for a number of common dopants with dose of $10^{15}$ cm$^{-2}$ and energy of 100 keV, (see Wittmann) and shown in Figure 3 a) below. As can be seen, Boron is predicted to give a very broad doping profile unsuitable for defining a *pn* junction, but suitable for providing a background p type doping to form the base. For the Group V elements, As, Sb, and P all give much sharper profiles, making them suitable for doping the emitter *n* type in order to form *pn* junction. The doping profiles for As and Sb are very shallow meaning that any junction would form too close to the surface of the structure. Having subjected the layer pre-transfer to ion implantation, differential capacitance-voltage profiling (see e.g. Schroder p. 65) was performed to characterize the *pn* junction assumed to form. Figure 3 b) shows the results of depth profiling, based upon C-V measurements, for a 2 µm silicon layer after ion implantation, showing a junction forming around 100 to 120 nm from the top surface, in good agreement with the predicted profile.

![Figure 3: pn junction formation; a) Predicted doping profiles for pn junctions formed in crystalline silicon by ion-implantation with $10^{15}$ cm$^{-2}$ dose and 100 keV energy for common dopants (Adapted from http://www.iue.tuwien.ac.at/phd/wittmann/node7). b) Measured doping profile for $^{31}\text{P}^+$ ion-implanted sample obtained using C-V profiling. As expected, we measured a steep junction formed 100-120 nm below the sample’s surface.](image)

In addition to be able to form a *pn* junction and to predict where the junction forms relative to the layer surface, the shape of the profile in the region will influence behavior of any photovoltaic device fabricated. By plotting of $1/C^2$ the ‘sharpness’ of the junction can be determined, in other words how rapidly does the doping density change in the vicinity of the junction using the relation

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_sN_B} (V_{bi} - V)$$

for a one-sided abrupt junction. From this measurement shown in Figure 4(a), the built-in potential $V_{bi}$ can be obtained directly from the intercept of the linear region at $1/C^2 = 0$, which give $V_{bi} = 0.67$ V. From this value, we can obtain directly the value for...
the width of the depletion region with no applied bias W(V=0) = 280 nm, which confirms the formation of a steep junction.

These results confirm that we have formed a good quality \( pn \) junction, the basic requirement for semiconductor based photovoltaic device, the only outstanding requirement is the ability to effectively absorb incident solar radiation. In order to check whether this was happening with the thin silicon layers, photocurrent spectroscopy measurements were taken. The results for a 2 \( \mu \)m thick layer with \( pn \) junction ~ 120 nm below the surface are given as a Tauc plot in Figure 4 b). Indicated by a dashed line is the band edge absorption, which as can be seen is ‘clean,’ in other words the absorption of photons with energy greater than the band gap is switched on rapidly with very little structure and a linear turn-on, implying good crystal quality and good absorption.

![Figure 4: Characterization of transferred flexible crystalline-silicon \( pn \) junction. a) C and \( 1/C^2 \) measurements allow the steepness of the junction formed by \( ^{31}\text{P}^+ \) implantation prior to substrate transfer to be determined, and b) Photocurrent spectroscopy displayed as a Tauc plot of the 2 \( \mu \)m thick \( ^{31}\text{P}^+ \) ion implanted flexible thin-film on PET substrate.](image)

The preliminary results for these layers are encouraging when the intended application is photovoltaics, since we have good well defined optical absorption and maintain the crystallinity of the silicon layer throughout the entire fabrication process. The thin layers that are being produced also ensure the structures are bendable to a small radius of curvature (~5 mm) with the crystallinity maintained throughout the bending process. It is not, however, enough to produce light absorbing \( pn \) junction, the processing of the layers into actual photovoltaic devices will now be briefly discussed.

**DISCUSSION AND FUTURE WORK**

The move to a more commercially viable production strategy for any thin silicon applications would need certain key questions answered. Firstly, a simple, reproducible fabrication process for synthesizing real devices from the flexible silicon layers would need to be developed. Typically for bulk solar cells the rear electrical contact is unpatterned and is simply a continuous Aluminum layer that has been fired to create a back surface field (Godlewski et al. 1973). For thin film silicon solar cells, a novel metal-induced crystallization of silicon has also been used to achieve a rear contact with the added benefit of improving the crystallinity of amorphous as-deposited silicon (Nast et al. 1999).

Solar cells made using the thin silicon transfer technique would seem to be limited to having an interdigitated contact scheme, an approach already successfully implemented
by Rogers and co-workers (Yoon et al. 2009). The firing of any metals used to make contact would necessarily have to be pre-transfer, as melting of the polymer substrate would be expected at typical anneal temperatures. This can be incorporated in the pre-transfer processing as in Yoon et al., though the choice of Au-Cr contacts seems curious as Au is a well-known ‘lifetime killer’ in silicon (Sah et al. 1969).

The inclusion of surface passivating layers has been demonstrated previously, with rear surface passivation provided through a back surface field (Yoon et al. 2009). This does introduce multiple high temperature diffusion steps into the processing sequence, complicating production and increasing cost. Low temperature, low cost passivation techniques would, therefore, be called for, for future development.

The other outstanding issue for flexible solar cells is the question of the effect of multiple bending events. As presented here and in other reports, the thin silicon layers show good structural integrity for bending down to roughly 5mm radius of curvature. However, the effects of repeated bending of the flexible structures would need to be done to imitate ‘roll out’ of a flexible solar panel as well as the roll up of the panel after charging has stopped. Also of interest is the performance of the panels under high bending conditions. Based on results reported for much thicker silicon solar cells (Blakers & Armour 2009) where minimal effect was seen for high bending conditions and repeated flexing events, there is every reason to be confident that the performance of these much thinner silicon devices would be only marginally impacted by repeated high bending events. Of interest also would be measurements performed for the devices under the added extreme of high operating temperatures.

CONCLUSION

In summary, preliminary results for a flexible and ultra-lightweight crystalline silicon-based platform produced through a novel fabrication process have been presented. Characterisation of the flexible silicon layers by confocal Raman microscopy, C-V profiling, and photocurrent spectroscopy, has revealed high crystal quality even under extreme bending conditions and the ability to define sharp and shallow pn junctions using ion implantation of Phosphorus. These structural properties of the fabricated flexible silicon should allow higher photovoltaic conversion efficiencies compared to more conventional amorphous silicon thin-film devices. Indeed, with the ability to fabricate crystalline silicon layers on polymer substrates, this novel platform should allow the flexibility and weight requirements associated with portable applications to be addressed in a superior manner to conventional structures. Some of the key processing challenges with moving this process to a more industrial footing have been briefly discussed along with some future measurements to assess how solar cells based on this technology would perform in the field.

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REFERENCES

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